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CONTROLLER TUNING FOR DISTURBANCE REJECTION ASSOCIATED WITH DELAYED DOUBLE INTEGRATING PROCESSES, PART II: I-PD CONTROLLER

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Abstract:-

An I-PD controller is investigated for disturbance rejection associated with delayed double integrating processes. The controller is tuned using the MATLAB optimization toolbox and five different error-based objective functions for process time delay between 0.1 and 5 s. The more suitable objective function for disturbance rejection with the I-PD controller used with the delayed double integrating process is assigned and the effect of the process time delay on the performance of the control system in the time domain is shown. The unit step disturbance input time response of the control system has a maximum value less than 0.431, time of maximum time response less than 1.01 s and a settling time less than 15 s for time delay ≤ 1 s. The simulation results using the I-PD controller are superior when compared with other disturbance rejection techniques based on using PD-PI and PIDF controllers.

Keywords: - *Disturbance rejection, delayed double integrating processes, I-PD controller, controller tuning.*

I. **INTRODUCTION**

Disturbance rejection is a performance requirement associated with feedback control systems. This performance depends on the type of process to be controlled and the type of controller or compensator used.

Ogawa and Katayama (2001) presented an I-PD setting formula to provide critically damped response to set point change for first-order lag process with dead time. They used a method of robust PID tuning by incorporating a constraint on the manipulated variable [1]. De Paor (2002) developed two stage procedure for stabilization and disturbance rejection for the control of integrating and unstable processes with time delay. They handled a number of illustrative examples showing the frequency response, unit step response and unit disturbance response [2]. Stogestad (2004) presented analytical rules for PID controller tuning to improve disturbance rejection for integrating processes. He considered delayed processes including non-integrating, single integrating and double integrating processes. He demonstrated the time response of the control system for set point and disturbance changes [3]

Zhang and Gao (2005) proposed a cost function to capture many practical design considerations. They studied tuning conventional PID controller and its variations for active disturbance rejection. They optimized the controller parameters using genetic algorithm [4]. Chatrattanawuth et. al. (2006) discussed a level control system using a fuzzy I-PD controller composed of Mamdani fuzzy I and Mamdani fuzzy PD controllers adjusted to desired control performances in transient and steady states [5]. Sridokbuap et. al. (2007) used an I-PD controller incorporating with PD controller to control an overhead crane system. Their simulation results has shown that the disturbance effect rejection was fast [6].

Goforth and Gao (2008) proposed ac active disturbance rejection control to reject hysteresis with unknown characteristics. They obtained promising results using simulation through application to typical hysteresis compensation problems in multiple of processes and applications [7]. Saravanakumar and Wahidabanu (2009) proposed a modified Smith predictor for controlling high-order processes with integral action and long deadtime. The controller was a PID one with integrator in the forward path and proportional and derivative parts in the feedback acting on the signal. They tuned the controller parameters to obtain a critically damped system for set point and load disturbance rejection performance [8]. Namazov and Basturk (2010) presented the design of a fuzzy control system to control the position of a DC motor. They used a crisp PD controller tunied using a simulink block and a fuzzy PD controller with different defuzzification methods. The fuzzy PD controller succeeded to reject a disturbance signal without further tuning whereby the crisp PD controller failed [9].

Rajinikanth and Latha (20012) proposed a method to tune an I-PD controller for time-delayed unstable process using Bacterial Foraging Optimization. They used ISE, IAE, ITSE and ITAE objective functions for a class of time-delayed unstable processes [10]. Prasad, Varghese and Balakrishnan (2012) optimized the parameters of I-PD controller using particle swarm intelligence for a first-order lag integrating plus time delayed model. They showed that the tuned I-Pd controller gave better performance compared with Ziegler-Nichols and Arvanitis tuning techniques [11]. Shiote and Ohmori (2012) proposed an adaptive I-Pd controller using augmented error method for SISO systems. They demonstrated the effectiveness of their method through simulation results [12]. Cbecinhas, Cunha and Silvestre (2013) proposed a nonlinear adaptive stable feedback controller to steer a quadrator vehicle along a predefined path. They presented experimental results where the quadrator was subject to external wind disturbance, showing the performance and robustness of the proposed controller [13].

Hassaan (2014) investigated the robustness of I-PD controller and two other controllers based on the P, I and D actions of PID controllers. He considered a variation of ± 20 % of the parameters of second-order-like processes and emphasized the robustness of the I-PD controller for set point change [14]. Mazumder and Dutta (2015) discussed the advantage of I-PD controller over the PID one. They showed that the I-PD controller will always be safer than the PID since it the suuden overshoot of the output variable [15]. Yazdanparast, Shahbazian, Alghajani and Abed (2015) proposed an active disturbance rejection control based on using asexual reproduction optimization to control the temperature of a nonlinear CSTR. They presented the controller design and tuned the parameters using particle swarm optimization and compared the performance of the control system with that using PSO(ADRC-PSO) and PID controllers [16].

II. CLOSED-LOOP CONTROL SYSTEM

The closed-loop control system incorporated an I-PD controller and a delayed double integrating process. The control system is a linear invariant one having two inputs, a reference input and a disturbance input. The block diagram of the system is shown in Fig.1 [11].

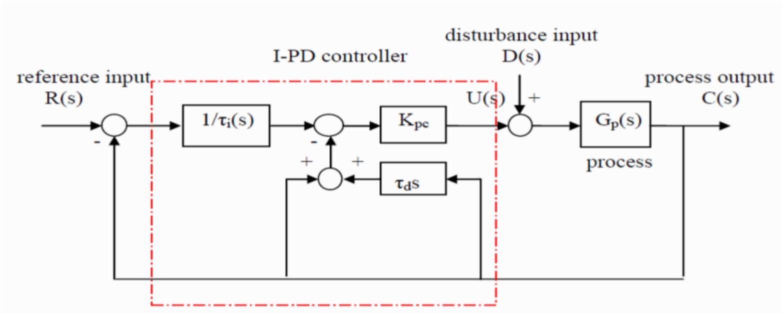


Fig.1 Block diagram of the control system with two inputs.

The closed-loop control system of Fig.1 has two inputs: the reference input R(s) and the disturbance input D(s). To investigate the effectiveness of the proposed controller in disturbance rejection, the reference input R(s) will be omitted from the block diagram and the disturbance input D(s) will replace it. The new block diagram of the control system is shown in Fig.2.

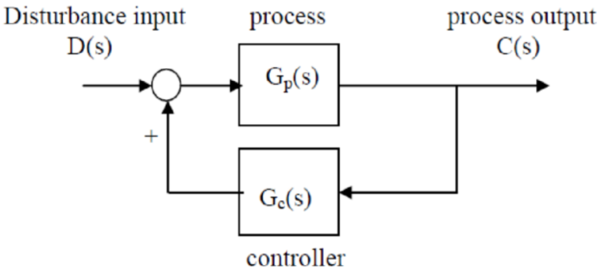


Fig.2 Block diagram of the control system with disturbance input.

The process is a delayed double integrating one having the transfer function:

$$G_p(s) = (K_p/s^2)\ \exp\ (-T_d s) \qquad (1)$$

Where K_p is the process gain and T_d is its time delay.
Using first-order Taylor expansion for the time delay expression [axp $(-T_d s)$], Eq.1 becomes [17]:

$$G_p(s) = (-T_d s + K_p) / s^2 \qquad (2)$$

The controller is an I-PD controller having the transfer function Gp(s) which is derived from Fig.1 as:

$$G_c(s) = -\ [K_{pc}/\ (\tau_i s)]\ (\tau_i \tau_d s^2 + \tau_i s + 1) \qquad (3)$$

Where K_{pc} is the proportional gain of the controller, K_i is its integral gain and K_d is its derivative gain.

The closed loop transfer function of the closed loop control system, C(s)/D(s) is given using the block diagram of Fig.2 and Eqs.2 and 3 by:

$$C(s)/D(s) = (b_0 s^2 + b_1 s)/\ (a_0 s^3 + a_1 s^2 + a_2 s + a_3) \qquad (4)$$

Where:
$b_0 = -\tau_i \tau_d$
$b_1 = \tau_i$
$a_0 = \tau_i - T_d K_{pc} \tau_i \tau_d$ a1 = Kpcτiτd –
TdKpc τi a2= Kpcτi - TdKpc $a_3 = K_{pc}$

III.CONTROLLER TUNING

Tuning of the I-PD controller allows adjusting the controller three parameters K_{pc}, τ_i and τ_d to achieve successful rejection of the input disturbance. The desired steady-state response in this case is zero. This means that the control system has to be less sensitive to disturbance input. This allows us to define an error function e(t) as the time response to its disturbance input d(t). That is:

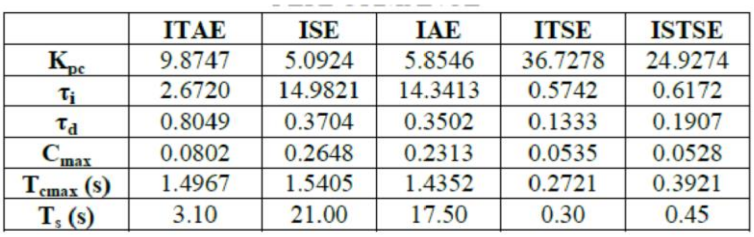
$$e(t) = c(t) \tag{5}$$

The controller tuning is performed using the error function of Eq.5 which is incorporated in an objective function to beminimized using the MATLAB optimization toolbox [18]. The objective functions used are [1922]:

ITAE: $\int t|e(t)|\, dt$ (6)
ISE: $\int [e(t)]^2\, dt$ (7)
IAE: $\int |e(t)|\, dt$ (8)
ITSE: $\int t[e(t)]^2\, dt$ (9)
ISTSE: $\int t^2[e(t)]^2\, dt$ (10)

The tuning results for a delayed double integrating process of unit gain and 0.1 s time delay with the specification parameters of a unit step disturbance input are given in Table 1.

Table 1 i-pd controller tuning and control system performance



	ITAE	ISE	IAE	ITSE	ISTSE
K_{pc}	9.8747	5.0924	5.8546	36.7278	24.9274
τ_i	2.6720	14.9821	14.3413	0.5742	0.6172
τ_d	0.8049	0.3704	0.3502	0.1333	0.1907
C_{max}	0.0802	0.2648	0.2313	0.0535	0.0528
T_{cmax} (s)	1.4967	1.5405	1.4352	0.2721	0.3921
T_s (s)	3.10	21.00	17.50	0.30	0.45

IV. DISTURBANCE REJECTION

The time response of the control system for a unit gain and 0.1 s time delay double integrating process using an I-PD controller using the five objective functions of Eqs.6 to 10 is shown in Fig.2. Fig.2 Unit disturbance system time response for a unit gain and 0.1 s time delay double integrating process. The effect of the time delay of the process on the dynamic performance of the control system when disturbance rejection is the objective and using the ISTE objective function is shown in Fig.3.

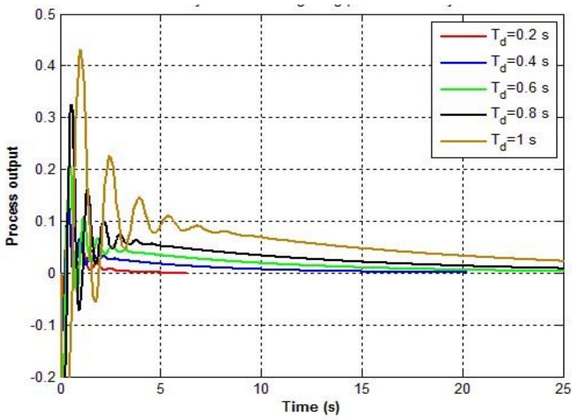


Fig.3 Effect of process time delay on the system disturbance time response using I-PD controller.

The effect of the process time delay on the maximum process output and settling time due to unit step disturbance **input using the ISTE objective function is shown in Fig.4.**

Fig.4 Effect of process time delay on the maximum process response and its settling time using I-PD controller.

V. COMPARISON WITH OTHER RESEARCH WORK

The results of the present research using an I-PD controller to reject the disturbance is compared with that of Hassaan using a PD-PI and Anil and Sree using a PIDF controllers for the same process of a delayed double integrating process having a unit gain and a unit time delay [23,24]. The unit step disturbance response of the control system is shown in Fig.5.

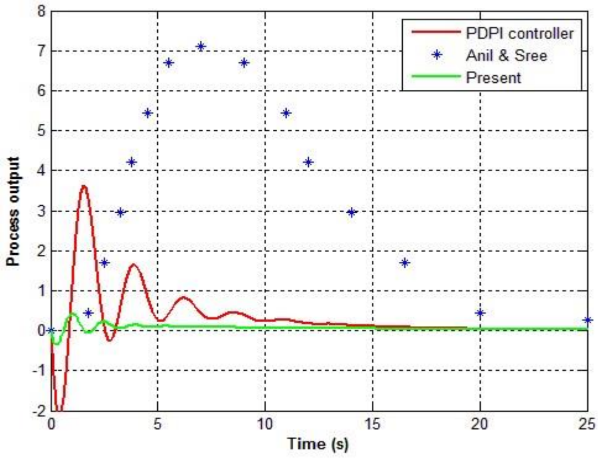
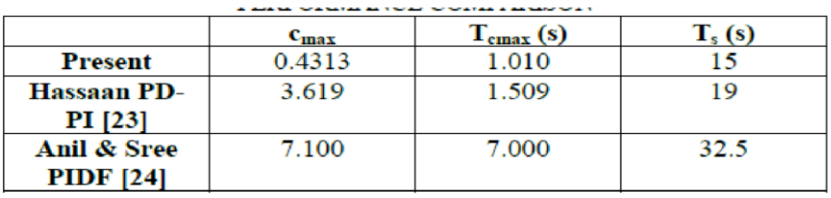


Fig.5 Comparison of the unit step disturbance.

The control system performance is compared in Table 2 between the present technique, PD-PI controller and the Anil and Sree PIDF technique.

Table 2 PERFORMANCE COMPARISON



	c_{max}	T_{cmax} (s)	T_s (s)
Present	0.4313	1.010	15
Hassaan PD-PI [23]	3.619	1.509	19
Anil & Sree PIDF [24]	7.100	7.000	32.5

The settling time, T_s is assigned as the time where the time response of the process violates and stays within a band of ± 0.05. This simply because the steady-state response of the control system in the dynamic case in hand is zero.

CONCLUSIONS

- An I-PD controller was used for disturbance rejection associated with delayed double integrating processes.
- A process time delay between 0.1 and 5 seconds was covered.
- The controller was tuned using the MATLAB optimization toolbox and five different objective functions were examined.
- The time response of the control system to a unit disturbance input had an oscillating nature for all the objective functions investigated.
- Better control system performance based on time response was obtained using the ISTE objective function.
- The effect of process time delay on the control system performance was investigated during disturbance rejection.
- The maximum output time response varied between 0.0535 and 0.4313 for process time delay between 0.1 and 1 s.
- The time at the maximum output time response varied between 0.272 and 1 seconds for the same time delay period.
- The settling time of the time response varied between 0.3 and 15 seconds for the same time delay period.
- Comparing with the research work using PD-PI and PIDF controllers, the maximum response for a unit disturbance input of a unit gain and unit time delay double integrating process was 0.4313 compared with 3.619 for PD-PI controller and 7.1 for PIDF controller.
- The time at the maximum time response was 1.01 s compared with 1.509 s for PD-PI controller and 7 s for PIDF controller.
- The settling time was 15 s compared with 19 s for PD-PI controller and 32.5 s for PIDF controller.

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