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THE PLATFORM MONITORING SYSTEM FOR WISDOM SHIPYARD BASED ON THE CCD SENSOR

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Abstract:-
Usually the settlement monitoring system was mainly applied in buildings, roads and so on in the city, which cannot meet the requirements of complex environments. While the train rail vibration monitoring, wind power platform settlement monitoring，etc are facing severe environmental interference. In order to ensure that rail, power tower platform and other field facilities to long-term and stable operation, there is a set of real-time monitoring system to monitor the settlement of the platform is particularly important. This paper proposes a new kind of high precision and micro displacement measurement technology based on laser and CCD devices, with the help of FPGA and MCU, we can complete the function of high-speed data acquisition and real-time monitoring easily. Compared with some traditional methods, this technology of measurement take great advantages in high-speed data acquisition, real-time performance, high-precision measurement and strong adaptability to complex environment, etc.

1. INTRODUCTION

The monitoring of the settlement includes the overall deformation monitoring of the sedimentation body, the inclination monitoring of the sediment body, and the monitoring of the external environment. The deformation and tilt of the sediment are the main monitoring contents, and the main basis for judging whether the platform settles [1]. At present, the common platform monitoring methods at Wisdom shipyard are: total station instrument monitoring method, displacement sensor detection method, Beidou/GPS detection method, laser monitoring method, etc. But the total station monitoring method is relatively short observation distance, cannot be long baseline measurement; Displacement sensor detection cannot measure objects that are difficult to access, the system adaptability is poor; Beidou/GPS detection method is expensive; Laser monitoring method, such as high real-time, high measurement accuracy, system adaptability and other advantages, is an effective way to monitor the settlement of the platform[2].

This paper presents a CCD-based platform settlement monitoring system design method. The monitoring method is a kind of laser monitoring method. The laser monitoring method is not affected by the weather and other factors. With the high resolution of the CCD device, it is easy to realize the high measurement accuracy of the monitoring system, the high system real time and the strong System adaptability. In addition, due to the low cost and high performance of the laser measurement method, it is easy to extend and apply the measurement method to other relevant settlement monitoring systems.

2. The System Composition and Basic Principles

2.1 The System Components

The system uses the characteristics of the laser and CCD high resolution, millimeter displacement (settlement) is easy to be accurately measured. The inclination of the base can be calculated using four different measuring devies[3].

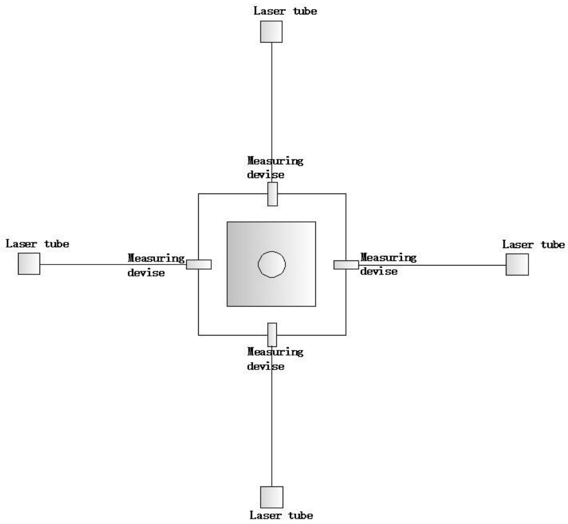

Figure 1: The Top view of pedestal platform settlement measuring device

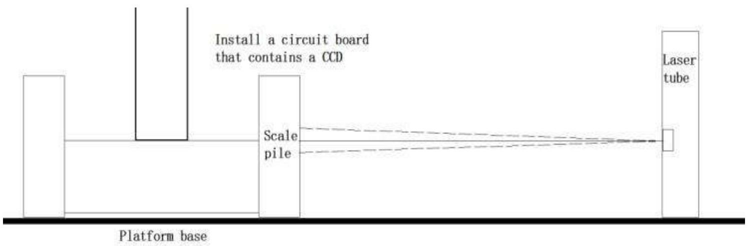

Figure 2: The Schematic diagram of laser side sedimentation

2.2 The Working Principle

The laser tube illuminates the CCD on the scale pile. According to the output data of the CCD, the position of the laser irradiation can be calculated. Normally, the position information of the CCD output should be a stable value (as indicated by the solid line in Figure 2). Offset will occur when the platform settles (as shown by the dotted line in Figure 2). According to the position the settlement information in one direction can be calculated. After the settlement information in four directions is aggregated, the settlement and tilt of the entire platform can be calculated to assess the health of the platform. At the same time, according to the measured settlement data to calculate the rate of change of the settlement and other information, and as a basis for forecasting the platform for a period of time the security situation.

The CCD captures the position information of the laser tube and outputs it to the signal preprocessing circuit. Then, the analog quantity is converted to digital quantity by ADC sampling. Data is stored in the FIFO after high-speed acquisition of the FPGA, the MCU later read the data from the FIFO and the corresponding processing [4].

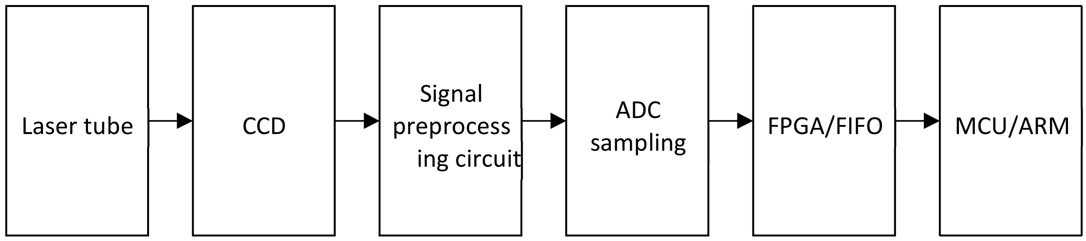

Figure 3: Functional block diagram of the measurement system

2.3 Introduction to The Basic Characteristics of CCD

CCD (Charge Coupled Devices), Chinese name for the charge-coupled device [1], with a wide response spectrum, responsive, high integration, low cost, easy maintenance and other characteristics, is a commonly used image sensor. CCD can be divided into two types: linear array CCD and area array CCD. The linear array CCD generally has a row of 500 to 10,000 light points, while the area array CCD has 500 × 500 to 20000 × 20000 light spots, each of the light points can independently measure the position of the response spectrum of light intensity, and Output in analog form.

CCD is generally used in scanners, fax machines, spectrometers and other applications, and this paper aims to use the special performance of the CCD to achieve settlement (fine displacement) monitoring.

3 The System Software Design

3.1 The FPGA Programming

This design requires the use of FIFO as a data cache, the ADC output high-speed data stored in the FIFO. When the MCU needs data, read the data from the FIFO. With the LPM (Library of Parameterized Modules) [5, 6] capabilities provided by Altera, high-performance, high-quality FIFO programs can be easily designed. The system needs to read the clock frequency lower than the write clock frequency, so the use of LPM function dual clock FIFO (DCFIFO, Dual-Clock FIFO).

3.2 Programming of STM32 and FPGA Communication

Communication mode between STM32 and FPGA, as shown in Figure 4, STM32 through the new data request bit to inform the FPGA to start data collection. When the STM32 busy flag is low, the FPGA processes the FIFO read request. When the FIFO read empty status bit is low, STM32 need to promptly revoke the FIFO request.

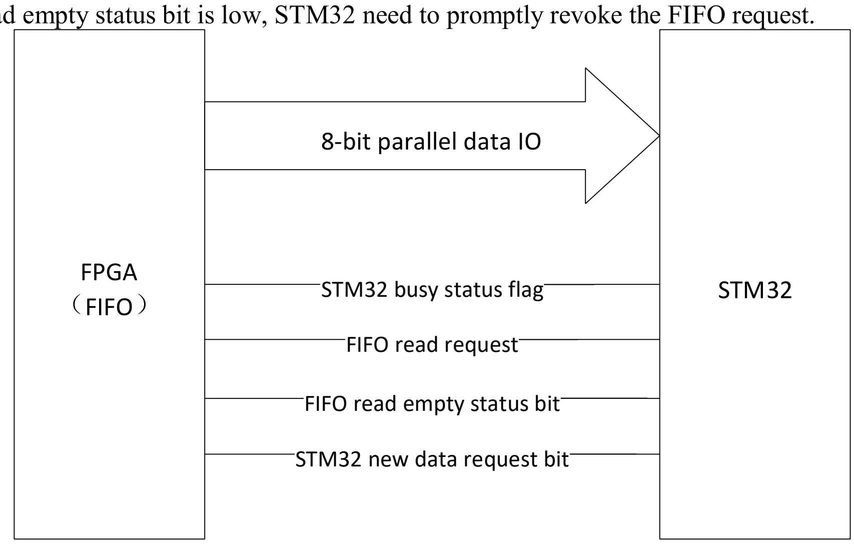

Figure 4: Block diagram of STM32 and FPGA communication

3.2 STM32 Programming

STM32 part of the main program to complete: FIFO data output read, data processing, send data to the host computer, man-machine interface display, human-computer interaction and other functions [7].

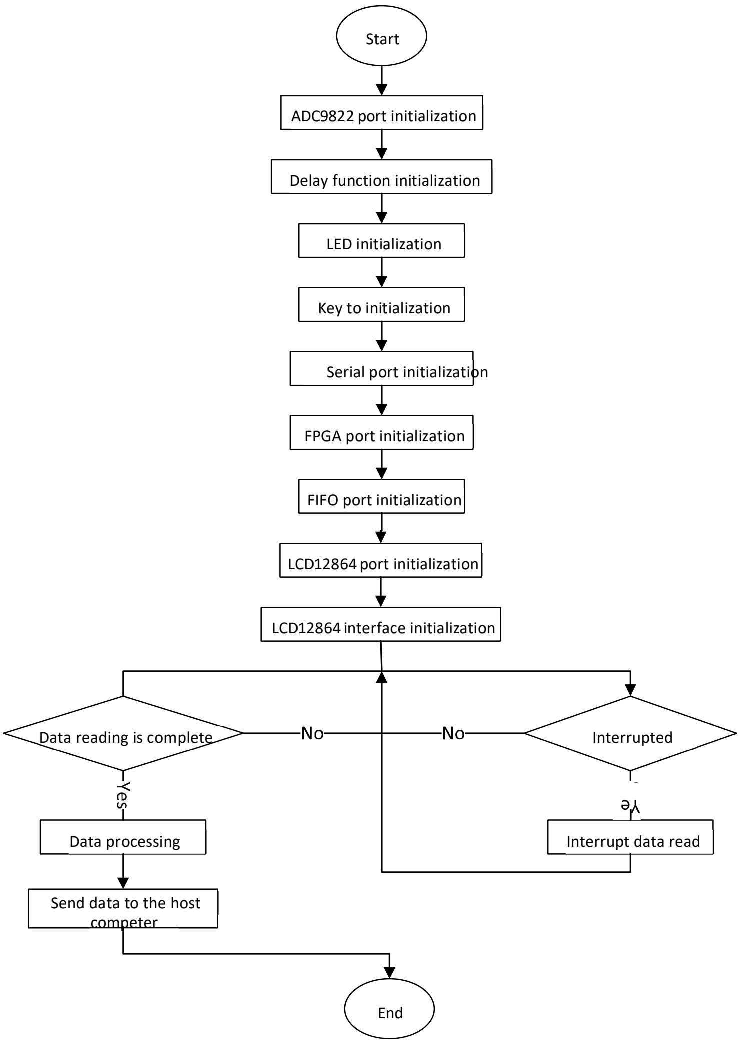

Figure 5: The whole flow chart of STM32 end system

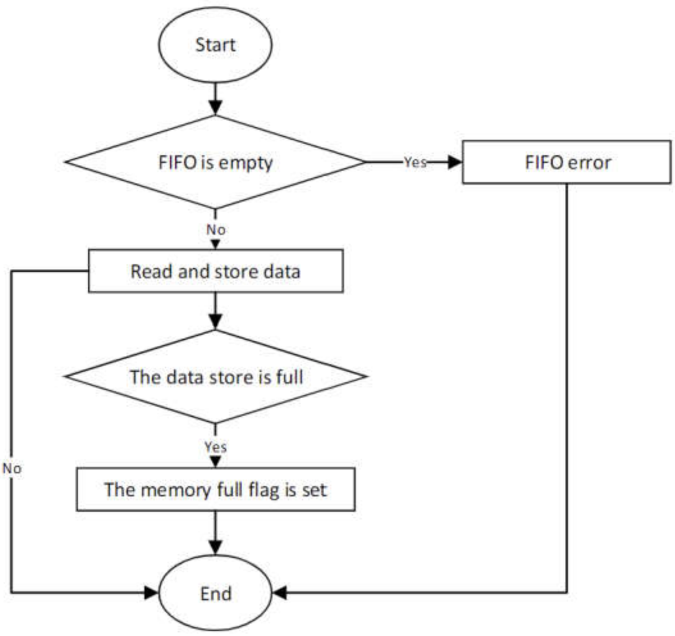

Figure 6: Flow chart for reading interrupt data

Figure 7: Data acquisition circuit board picture

Figure 8: Data processing circuit board picture

4. The Experiment and Analysis

4.1 The Output Image Processing

As the CCD output waveform is a negative logic image, the default no signal output is about 2.5V constant voltage, when there is a signal output will be based on the response of the light output of a certain negative voltage, the stronger the stronger the light The stronger the voltage. Since the CCD is more sensitive to light intensity, it is necessary to add a polarizer to attenuate the light intensity and filter out other disturbances. The final CCD output is the sum of the resulting negative voltage plus a constant voltage of about 2.5V. Since the negative voltage range is 0-600mV, no negative voltage is generated on the overall final output.

Observing the oscilloscope measurements of the CCD output signal, the lowest voltage across the waveform period is the position of the laser beam, but the falling edge and the rising edge of the effective output are not particularly steep due to the divergence effect of the CCD itself and the outer glass. In order to more intuitive display of data, extract the data processing through MATLAB for drawing display. Since the output pattern of the CCD is a "negative logic" output, all the 0 outputs (dark dots) are all changed to 0 and the image is inverted before the display. While filtering the edge effect on both sides of the lowest point, so that the rising edge and falling edge of the processed waveform are steeper and the display is more pronounced.

4.2 Data Analysis

The expected measurement accuracy of this system is 1mm, the following were analyzed day and night measurement data, and calculate the corresponding measurement error, to verify whether it can achieve the desired results and meet the actual requirements. Since the selected CCD has a total of 3648 effective pixels, the size of each pixel is 8 □m × 200 □m, and the effective measurement area of the CCD is 37mm, so the spacing between two pixels is 2 □m. For convenience of calculation and data analysis, it is assumed in the following discussion that the size of each pixel is 10 □m × 200 □m and the spacing between two pixels is 0.

For convenience of comparison, the measurement will be 0-37mm effective measurement area corresponding to 1-3648 effective pixels. The center position of the CCD, that is, the position of 18.5mm as the center position, respectively, up and down to do the slight displacement, compared with the actual measured value and the theoretical value, and calculate the corresponding displacement error.

Table 1: The actual displacement of 1mm measurement data analysis

(Actual displacement: 1mm ;Theoretical data point offset: 99)

Time	Numbering	Actual data point offset	Data point error (s)	Measuring displacement (mm)	Displacement error	Average error
Day	1	97	-2	0.98382	2.020%	3.704%
	2	94	-5	0.95340	5.051%	
	3	96	-3	0.97368	3.030%	
	4	93	-6	0.94325	6.061%	
	5	95	-4	0.96354	4.040%	
	6	97	-2	0.98382	2.020%	
Night	7	99	0	1.00000	0.000%	0.673%
	8	101	2	1.02439	2.020%	
	9	99	0	1.00000	0.000%	
	10	98	-1	0.99397	1.010%	
	11	100	1	1.01425	1.010%	
	12	99	0	1.00000	0.000%	

Table 2: The actual displacement of 2mm measurement data analysis

(Actual displacement: 2mm ; Theoretical data point offset: 197)

Time	Numbering	Actual data point offset	Data point error (s)	Measuring displacement (mm)	Displacement error	Average error
Day	1	194	-3	1.96765	1.523%	1.438%
	2	193	-4	1.95750	2.030%	
	3	196	-1	1.98793	0.508%	
	4	194	-3	1.96765	1.523%	
	5	195	-2	1.97779	1.015%	
	6	193	-4	1.95750	2.030%	
Night	7	197	0	2.00000	0.000%	0.432%
	8	199	2	2.01836	1.015%	
	9	197	0	2.00000	0.000%	
	10	198	1	2.00822	0.508%	
	11	196	-1	1.98793	0.508%	
	12	198	1	2.00822	0.508%	

Observe the comparison of measurement data, found that the daytime error is slightly larger than the night. Mainly because of strong light intensity during the day, compared to the night, the interference factor is more. But even the largest error is only 3.704%, enough to meet the practical application requirements, and in the measurement device after black box processing will reduce the system during the day of measurement error.

5. Conclusions

An optical non-contact settlement (displacement) measurement design based on CCD is proposed in this paper, which is characterized by high measurement accuracy, high stability and low cost relative. The system uses the ADC to sample the output signal of the CCD, and the FIFO is implemented by the FPGA for data temporary storage, and then the data is sent to the STM32 for data processing and display. And all the device driver timing are generated by the FPGA. The experimental requirements can be achieved by experimentation. Compared with the traditional settlement (displacement) measurement schemes, we demonstrate the effectiveness of the proposed approach. The results show that this system has better performance with lower errors, higher accuracy, and higher versatility.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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References

[1]. Steve Holland. An Overview of CCD Development at Lawrence Berkeley National Laboratory [J]. Lawrence Berkeley National Laboratory，2002.

[2]. STMicroelectronics. STM32F103VCT6 Datasheet[R]. STMicroelectronics group of companies，2009.

[3]. Altera Corporation. Cyclone IV FPGA Device Family Overview [R]. Altera Corporation，2014.

[4]. Analog Devices, Inc. Complete 14-Bit CCD/CIS Signal Processor [R]. Analog Devices, Inc，1999.

[5]. Altera Corporation. Single- and Dual-Clock FIFO Megafuction User Guide [R].Altera Corporation，2007.

[6]. Hyoung-Kook Kim，Laung-Terng Wang，Yu-Liang Wu，Wen-Ben Jone. Testing of Synchronizers in Asynchronous FIFO[J]. Department of Electrical and Computer Engineering，University of Cincinnati，Cincinnati，OH 45221，USA，2013.

[7]. STMicroelectronics. STM32F10xxx advanced ARM-based 32-bit MCUs Referencemanual[R]. STMicroelectronics group of companies， 2014. 788-820.

[8]. Mark I. Montrose. Printed Circuit Board Design Techniques For EMC Compliance (Second Edition)[M]. John Wiley & Son， Inc.， 2006. 80-84.

[9]. Analog Devices, Inc. 300MHz, 1mA Current Feedback Amplifier AD8011 [R].Analog Devices, Inc， 2000.